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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,253	10/29/2003	Alex Fishman	15436.253.77.1	7077

22913 7590 02/24/2005

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EXAMINER	
WACHSMAN, HAL D	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

CT

Office Action Summary	Application No.	Applicant(s)	
	10/696,253	FISHMAN ET AL.	
	Examiner	Art Unit	
	Hal D. Wachsman	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 2 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☒ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-22* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This application is in condition for allowance except for the following formal matters:

a) The declaration provides the post office addresses of the inventors but does not indicate that these are the residences too. In addition, there are separate pages, each of these separate pages containing one inventors signature and date, however on each of these pages there is no other text of the declaration, and thus it is not clear that each and every inventor is attesting to the statements of the declaration. Appropriate correction is required.

b) The bibliographic data on PALM for this application as well as the Cross-Reference To Related Applications on page 1 of the specification, indicate a claim for priority to provisional applications 60/422,598, filed October 31, 2002, 60/423,968 filed November 5, 2002 and 60/423,959, filed November 5, 2002. However, the instant application is also a CIP of 10/285,082 and 10/285,081 both of which were filed October 31, 2002. As provisional applications 60/423,968 and 60/423,959 were both filed on November 5, 2002 which is after the CIP parent cases filing date, there is ambiguity with respect to exactly what is the basis for priority here with respect to those two provisional applications. In addition, the Examiner notes that provisional application 60/423,968 has a different title than the instant application. Appropriate explanation/correction is required.

c) The Cross-Reference To Related Applications on page 1 of the specification does not provide the current status of U.S. application serial numbers 10/285,082 and 10/285,081. Appropriate correction is required.

d) The Abstract has beneath it "W:\15436..." which should be deleted.

e) The use of the trademarks Agilent Digital Communication Analyzer (page 4), Motorola 8-bit processor (page 12) and EXPO Optical Test System IQ-203 have been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

f) The Examiner respectfully notes that a period is missing at the end of paragraph 002 on page 1 of the specification.

g) Claims 1-22 are objected to under 37 C.F.R. 1.75(a) for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 1, line 5, cites "said first sequence" however the antecedent. basis is "first sequence of bits". This same type of problem also occurs in claim 11, lien 5. Claim 1, lines 11-12, cite "...said jitter tolerance of said optoelectronic device is determined by reference to comparison" but the claim does not particularly point out how exactly the comparison is being used here to determine the jitter tolerance.. The preamble of claim 7 first states "In a system for measuring....said system comprising..." however before the beginning of the body of the claim the preamble states "..a method for computing the jitter tolerance..." which as written creates some ambiguity in the preamble with respect to whether this is a system claim or a method claim. This same type of problem also occurs in the preamble of claim 18. Claim 7, line 8, cites "said bits"

which it appears should be "said first sequence of bits". This same type of problem also occurs in claims 8 and 9. The last line of claim 7 cites "using said bit error rate to determine said jitter tolerance" which does not particularly point out how exactly the bit error rate is being used to determine the jitter tolerance. This same type of problem also occurs in the last line of claim 18. Claim 11, lines 12-13, cite "...said signal attenuation tolerance of said optoelectronic device is determined by reference to said comparison" which does not particularly point out how exactly the comparison is being used to determine the signal attenuation tolerance. Claim 13, line 1, cites "said delay" however the antecedent basis is "delay circuit". This same type of problem also occurs in claim 14, line 3, claim 15, line 1, claim 16, line 3. Claim 14, line 4, cites "said bit error rate" which lacks clear antecedent basis. This same type of problem also occurs in claim 16, line 4. Claim 16, lines 5 and 6, cite "each of said plurality of data points" which it appears should be "each data point of said plurality of data points". This same type of problem also occurs in claim 22, line 5. Claim 18, line 8, cites "said bits" however the antecedent basis is "first sequence of bits". The examiner asks the applicant to better claim the limitations cited above. While the examiner understands the intentions of the applicant he feels confusion could be drawn from the limitations cited above. Appropriate correction is required.

Prosecution on the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

A shortened statutory period for reply to this action is set to expire **TWO MONTHS** from the mailing date of this letter.

2. The following references are cited as being art of general interest: "Jitter testing for gigabit serial communication transceivers" (Yi Cai et al.) which disclose the tolerance level of Sonet transceivers with respect to attenuation and jitter, Dalmia et al. (5,835,501) which disclose a built-in test scheme for a jitter tolerance test of a clock and data recovery unit, Bonneau et al. (6,834,367) which disclose the use of a pattern generator, serializer and deserializer, and Sorna (US 2003/0223526 A1) which discloses the measurement of jitter tolerance.

3. Claims 1-6 are allowable over the prior art because the prior art does not disclose or suggest: the transmission of a first sequence of bits to a delay circuit, each of the bits subject to a delay prior to being transmitted to an optoelectronic device and comparison circuitry that receives a second sequence of bits, which the optoelectronic device derives from the first sequence of bits, the jitter tolerance of the optoelectronic device being determined from a comparison of the two sequence of bits.

Claims 7-10 are allowable over the prior art because the prior art does not disclose or suggest: delaying a first sequence of bits and individually transmitting the bits to an optoelectronic device; transmitting a second sequence of bits derived from the first sequence of bits from the optoelectronic device to a controller and using a bit error rate derived from a comparison of the two sequences of bits to determine the jitter tolerance.

Claims 11-17 are allowable over the prior art because the prior art does not disclose or suggest: the transmission of a first sequence of bits to a delay circuit and then to an attenuator that performs an attenuation of the power level of the first sequence of bits before being sent to an optoelectronic device and comparison circuitry that receives from the optoelectronic device a second sequence of bits, that was derived from the first sequence of bits, in which a signal attenuation tolerance is determined from a comparison of the two sequences of bits.

Claims 18-22 are allowable over the prior art because the prior art does not disclose or suggest: delaying a first sequence of bits and individually transmitting the bits to an optoelectronic device; transmitting a second sequence of bits derived from the first sequence of bits from the optoelectronic device to an optical attenuator and using a bit error rate derived from a comparison of the two sequences of bits to determine the attenuation tolerance.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal D. Wachsman whose telephone number is 571-272-2225. The examiner can normally be reached on Monday to Friday 7:00 A.M. to 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hal D Wachsman
Primary Examiner
Art Unit 2857

HW
February 20, 2005